What is claimed is:

1. An asynchronous transfer mode ("ATM") integrated access device comprising:

a first input configured to provide a first plurality of ATM cells at a first ingress rate to

a first input buffer;

a second input configured to provide a second plurality of ATM cells at a second ingress rate to

a second input buffer;

an output buffer configured to queue ATM cells for transmission on a physical network interface at an egress rate;

a programmable timer programmed to generate a cell tick period according to the egress rate;

an arbiter controlled by the programmable timer, the programmable timer enabling the arbiter to read a cell from either the first input buffer or the second input buffer to the output buffer each cell tick period.

2. The ATM integrated access device of claim 1 wherein the egress rate is at least twenty times greater than the first ingress rate.

3. The ATM integrated access device of claim 1 wherein the egress rate is at least two hundred times greater than the first ingress rate.

4. The ATM integrated access device of claim 1 wherein the egress rate is no more than 1.1 times the second ingress rate.

5. The ATM integrated access device of claim 1 wherein the egress rate is at least twenty times greater than the first ingress rate and the egress rate is no more than 1.1 times greater than the second ingress rate.

6. The ATM integrated access device of claim 1 wherein the arbiter is configured to read a first ATM cell in the first input buffer before reading a second ATM cell from the second input buffer.

7. The ATM integrated access device of claim 1 wherein the first plurality of ATM cells are provided by a segmentation and reassembly unit operating according to ATM adaptation layer 1 protocol.

8. An asynchronous transfer mode ("ATM") integrated access device comprising:

a first input from a first segmentation and reassembly unit operating under ATM adaptation layer 1 protocol, the first input providing a first plurality of ATM cells at a first ingress rate to

a first input buffer;

a second input providing a second plurality of ATM cells to

a second input buffer;

an output buffer configured to queue ATM cells for transmission on a physical network interface at an egress rate, the egress rate being at least twenty times the first ingress rate;

a programmable timer programmed to generate a cell tick period according to the egress rate;

an arbiter enabled by the programmable timer each cell tick period to read a first cell from the first input buffer to the output buffer if the first cell is present in the first input buffer and, if no first cell is present in the first input buffer, to read a second cell from the second input buffer to the output buffer.

9. A method of routing asynchronous transfer mode ("ATM") cells through an ATM integrated access device, the method comprising:

providing an egress rate of the ATM integrated access device to a processor;

calculating a cell read period according to the egress rate;

programming a programmable timer with the cell read period, the programmable timer

enabling a read of an ATM cell from an input buffer to an output buffer each cell read period.

10. The method of claim 9 wherein the calculating step includes

determining a cell egress rate,

rounding the cell egress rate down to a next lowest integer cell egress rate, and

taking the inverse of the next lowest integer cell egress rate to calculate the cell tick period.

11. The method of claim 10 wherein the determining step determines the cell egress rate according to a physical network interface cell rate.

12. The method of claim 9 wherein the cell read period is a cell tick period minus an overhead period.

13. The method of claim 9 further including steps, after the enabling step, of

checking a high-priority input buffer and, if a high-priority cell is present, reading the high-priority cell to an output buffer, and if a high-priority cell is not present, then

checking a lower-priority input buffer and, if a lower-priority cell is present,

reading the lower-priority cell.

14. The method of claim 13 further comprising steps, after the reading the lower-priority cell step, of

determining if the lower-priority cell is an idle cell, and if the lower priority cell is an idle cell, then

discarding the lower-priority cell.

15. A method of routing asynchronous transfer mode ("ATM") cells through an ATM integrated access device, the method comprising:

providing an egress rate of the ATM integrated access device to a processor;

determining a cell egress rate;

rounding the cell egress rate down to a next lowest integer cell egress rate;

taking the inverse of the next lowest integer cell egress rate to calculate the cell tick period;

programming a programmable timer with the cell read period; and

enabling an arbiter to read an ATM cell from an input buffer to an output buffer each cell read period.